REMARKS

These remarks are in response to the Non-Final Office Action mailed May 15, 2007 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1-20 stand rejected. Claims 1, 16, and 18 have been amended to clarify various aspects of the present invention. Support for these amendments can be found at paragraphs 18, 19, 25, and throughout the Applicants' specification. No new matter has been introduced. Claims 1-20 remain pending. Claims 1-20 are rejected.

Within these remarks the Applicants may address more than one claim or more than one element from different claims concurrently. This treatment of claims and/or elements of claims is solely to track the manner in which the rationale for rejecting the claims is set forth in the Office Action, e.g., where similar or the same citations are applied against more than one element from different claims. Though one or more elements of different claims may refer to similar or the same subject matter, the concurrent treatment of, or use of the same reasoning in support of, two or more claims and/or elements of different claims does not, in and of itself, imply that such claims and/or elements refer to the same subject matter or recite the same feature.

35 U.S.C. § 103

Claims 1-14 and 16-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,345,378 to Joly et al. (Joly) in view of U.S. Patent No. 6,374,205 to Kuribayashi et al. (Kuribayashi), in view of U.S. Patent No. 6,173,434 to Wirthlin et al. (Wirthlin), in further view of U.S. Patent No. 6,968,487 to Bryant et al. (Bryant).

Claims 1, 16, and 18 recite "create a netlist of objects specifying each object for the target hardware architecture, wherein the target hardware architecture is a field programmable gate array". Joly does not teach or suggest such a feature. Joly is directed to circuit design for an Application Specific Integrated Circuit (ASIC). Generally, circuit structure is created within an ASIC in consequence of the circuit design. Such circuit structure does not exist apart from the circuit design itself as is the case with programmable structures available within a field programmable gate array (FPGA).

The netlist of objects recited in claims 1, 16, and 18 specifies objects for the target hardware architecture, i.e., objects of the FPGA apart from the circuit design to be implemented therein. In illustration, this netlist of objects is compared with the objects used by the circuit design to determine unused objects of the target hardware architecture. Joly does not teach or suggest any netlist against which a circuit design can be compared to determine unused objects of the target hardware architecture as recited in claims 1, 16, and 18. Such is the case as structure is created from a circuit design for an ASIC and is not "pre-existing" as is the case with an FPGA.

Claims 1, 16, and 18 further recite "identify objects specific to the target hardware architecture that are repeated to identify potential dummy objects". The Office Action contends that Joly teaches this feature and cites several passages discussing the removal of gates from a circuit design. As noted in Applicants' prior response, it appears that the Office Action is drawing an analogy between the removal of gates and the identification of potential dummy objects. The Applicants disagree with this characterization of Joly.

The gates discussed in Joly are removed from the circuit design. Objects of the netlist that are replaced with dummy objects, as recited in claims 1, 16, and 18, are not removed. Rather, the functional hardware description language is removed from the object. Each such object remains in the netlist and is simulated as recited in the "simulating" element. For these reasons, the analogy of the removal of gates to the identification of potential dummy objects is inappropriate.

The Office Action concedes that Joly does not teach or suggest simulating the modified netlist. In fact, Joly is directed entirely to synthesis, not simulation. Notwithstanding, it is asserted that Kuribayashi teaches this feature. Kuribayashi, however, does not teach or suggest that the modified netlist is simulated "by simulating each object of the modified netlist inclusive of each dummy object, wherein for each dummy object, a signal provided to the dummy object is fed through the dummy object unchanged" as recited in claims 1, 16, and 18.

Kuribayashi actually teaches away from this feature. At column 4, lines 45-53, Kuribayashi states:

> [t]he method may include the step of deleting at least one of resistors, capacitors, inductance elements, control voltages, and diodes connected to MOS transistors that are not extracted from circuit data. This technique allows not only transistors but also elements such as resistors, capacitors, inductance elements, control voltages, and diodes connected to the transistors to be reduced.

The above passage is clear that Kuribayashi deletes elements of the circuit design. By comparison, claims 1, 16, and 18 recite that each object and dummy object of the netlist is simulated. Objects are transformed into dummy objects and simulated, not deleted as is the case with Kuribayashi. Kuribayashi does not teach or suggest that each object and dummy object of the netlist is simulated. Kuribayashi purges circuit elements rather than rendering objects as dummy objects and simulating the objects. As noted in Applicants' specification, all elements of an object of an FPGA are to be simulated. Rendering an object as a dummy object addresses this situation in that the object remains in the netlist for simulation. Simulation time of the dummy object is reduced through reduction of code.

Further, Kuribayashi, like Joly, is directed to ASICs. From the above passage, for example, Kuribayashi clearly manipulates a circuit in terms of individual components, i.e., transistors, resistors, etc., whereas the Applicants' recited features function on an object level in reference to FPGA structures, e.g., configurable logic blocks.

Neither Joly, Kuribayashi, nor Wirthlin teaches or suggests "replac[ing] at least one object in the netlist of objects for the target hardware architecture that is also specified in the list of unused objects and which is identified as a potential dummy object with an appropriate dummy object to form a modified netlist by removing functional hardware description language from the object". It is asserted, however, that Bryant does. Bryant, like Joly, is not directed to simulation. Instead, Bryant is directed to utilizing built in self test (BIST) functions of the physical integrated circuit.

Regardless, Bryant teaches that registers can be inserted into a user circuit design. The registers do not perform as part of the user circuit and facilitate BIST functions of the physical integrated circuit. Claims 1, 16, and 18 recite that functional hardware description language is removed from an object to form the dummy object. This differs significantly from the insertion of a register into the circuit design.

The removal of functional hardware description language from an object results in an object that, while still simulated, has less code to be executed during simulation. Bryant does not modify objects of a netlist by removing functional hardware description language. In the best case, inserting dummy registers into the circuit design, as suggested by Bryant, would not decrease the speed of simulation as does removal of code from objects. In the worst case, however, insertion of registers may result in increased code to execute, thereby slowing simulation.

Claim 11 references several features that are similar to those already addressed herein. Accordingly, claim 11 is believed to be both novel and non-obvious over Joly, Kuribayashi, Wirthlin, Bryant, or any combination thereof for the same reasoning as set forth above. The remaining claims are believed to be allowable in view of their own merits and further by virtue of their dependence upon underlying base claim(s) discussed above.

In closing, the Office Action appears to adopt a piecemeal approach that neglects the claims as a whole. As one example, while a particular number of references being applied in a 35 U.S.C. § 103(a) rejection may not be dispositive of a piecemeal approach to the claims, the need for four references in sustaining the 35 U.S.C. § 103(a) rejection may serve as an indication of a piecemeal approach. No less than five references have been cited in support of the 35 U.S.C. § 103(a) rejection of claim 15.

Further, of the four primary references, two (Joly and Kuribayashi) appear to be directed to ASICs, not FPGAs. This neglects aspects of FPGA architecture and simulation referenced in the Applicants' specification and claims that are not shared with ASICs. Additionally, three of the four references (Joly, Wirthlin, and Bryant) are

not directed to simulation at all, but rather to different aspects of synthesis, hardware testing using BIST structures, and dynamically reconfiguring an FPGA. This neglects the differences between circuit implementation and simulation, e.g., the discussion dealing with the differences between removing functional language of objects and insertion of dummy registers described by Bryant.

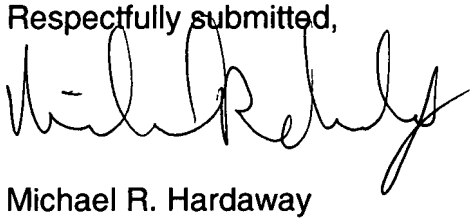
As neither Joly, Kuribayashi, Wirthlin, Bryant, U.S. Patent No. 6,857,110 to Rupp et al., nor any combination thereof, teaches or suggests the Applicants' invention as claimed, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-20 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,



Michael R. Hardaway
Attorney for Applicants
Reg. No. 52,992

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 14, 2007.

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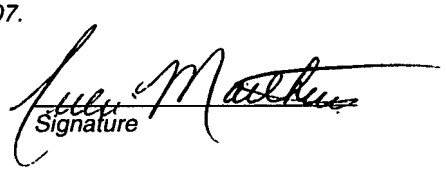

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